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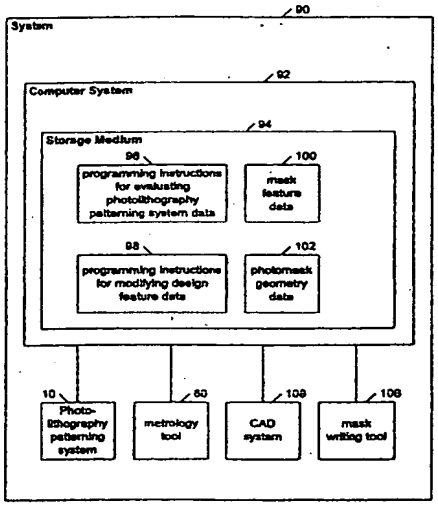
(54) Title: SYSTEM, METHOD AND PHOTOMASK FOR COMPENSATING ABERRATIONS IN A PHOTOLITHOGRAPHY PATTERNING SYSTEM



(57) Abstract: A method, system, and photomask is used to compensate for aberrations in a photolithographic patterning system, and to improve the overall process control of substrate features formed by a compensated photolithography mask. The photolithography mask is derived such that substrate features are corrected to compensate for photolithography patterning system aberrations. Test features contained on a photomask can be printed in a photoresist located on an upper surface of a semiconductor substrate by a photolithography patterning system. Images of the test patterns are evaluated by a metrology tool, for example, measured by a scanning electron microscope, and then assessed to characterize the system aberrations. Characterization of the aberrations indicates the size and location of an aberration-affected area, and the aberrations' effects on various types of design features. The design features which would be affected by the aberrations are modified by changing their size(s) and/or shape(s) to form mask features configured to compensate for the aberration-induced distortions.

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TITLE: SYSTEM, METHOD AND PHOTOMASK FOR COMPENSATING ABERRATIONS IN A PHOTOLITHOGRAPHY PATTERNING SYSTEM

BACKGROUND OF THE INVENTION

1. Technical Field

This invention relates to semiconductor processing and, more particularly, to a method, system, and photomask for compensating for aberrations in a photolithography patterning system.

2. Background Art

Fabrication of integrated circuits upon semiconductor substrates ("wafers") involves numerous processing steps. For example, the fabrication of a metal-oxide-semiconductor ("MOS") integrated circuit includes the formation of trench isolation structures within a semiconductor substrate to separate each MOS field-effect transistor ("MOSFET") that will be made. The semiconductor substrate is typically doped with either n-type or p-type impurities. A gate dielectric, typically composed of silicon dioxide, is formed on the semiconductor substrate. For each MOSFET being made, a gate conductor is formed over the gate dielectric and a source and drain are formed by introducing dopant impurities into the semiconductor substrate. Conductive interconnect lines are then formed to connect the MOSFETs to each other and to the terminals of the completed integrated circuit. Modern high-density integrated circuits typically include multiple interconnect levels to provide all of the necessary connections. Multiple interconnect levels are stacked on top of each other with intervening dielectric levels providing electrical insulation between interconnect levels.

During integrated circuit fabrication, various structures of the circuit are patterned. These structures may include trench isolation structures, gate conductors, and interconnect lines. Typically, optical photolithography is used in performing the patterning. Photolithography is a process whereby a pattern may be transferred from a photomask onto the semiconductor topography. However, prior to transferring a pattern from a photomask to a wafer surface, it is necessary to create a pattern on the photomask. One of the earliest steps in integrated circuit production is translating a circuit design into a layout design. A layout design defines the size and shape of the circuit features for each processing layer. Computer aided design packages exist which enable design layout by, among other things, taking into consideration the design rules within and between the various processing layers. Once a layout design is completed, a photomask (or a set of photomasks) may be fabricated from, e.g., a pattern generation ("PG") of the CAD layout design.

A photomask is created by writing photomask geometry data to a photoblank using a photomask writing system, or PG. A photoblank substrate is typically quartz, but may be soda lime, borosilicate, or white crown. The photoblank may vary in size. For example, it may be from 2 to 7 inches square or it may have a diameter of 7.25 inches. A typical photoblank is a quartz plate with a layer of chrome on one side. The chrome is generally covered with an anti-reflective coating and a photosensitive material, often called photoresist. A photomask writing system may be, for example, an electron beam ("e-beam") tool or a laser tool which transfers the desired circuit features to the photoblank by exposing the photoresist. The exposed photoresist may then be removed with a developer, assuming a positive photoresist is used. The photoblank is subsequently etched to remove the anti-reflective coating and chrome wherever the resist has been removed. A final step in creating the photomask is stripping the remaining photoresist from the photoblank.

As stated above, photomasks are typically required for photolithography. Photolithography begins by applying photoresist as a thin film to an upper surface of the wafer. Light is then projected onto the photoresist through a photomask which contains clear and opaque features that define the pattern to be created in the photoresist. If a positive photoresist is used, the portions of the photoresist exposed to the light are rendered soluble in a specific solvent, often called developer. If a negative photoresist is used, the portions of the photoresist exposed to the light are rendered insoluble in developer. After the developer removes soluble portions of the photoresist, the remaining photoresist forms a mask. The resulting mask may be used in patterning layers of the wafer underneath the photoresist. For example, the photoresist may be used to protect the covered portions of the semiconductor substrate while the exposed portions of the semiconductor substrate are etched. Alternately, the resulting mask may also be used in blocking implants into the wafer layers beneath the photoresist. For example, the photoresist may be used to shield the covered portions of the substrate while the exposed portions are implanted with impurities.

One commonly used photolithographic patterning system is the step and repeat projection system in which the photomask can pattern only a portion of the photoresist. A step-and-repeat system projects a pattern of the photomask onto a portion of the semiconductor substrate. The step-and-repeat system then moves, or "steps", the semiconductor substrate and projects the pattern of the photomask onto a different portion of the semiconductor substrate. The entire photomask field may be projected in a single flash while the photomask plane and the wafer plane are stationary relative to one another. This type of step-and-repeat system is commonly referred to as a "stepper". Another type of step-and-repeat system is commonly referred to as a "scanner". When a scanner is used, a portion of the photomask field is projected while the photomask plane and the wafer plane move with respect to the exposing radiation. Either process is repeated until a photomask's pattern has been projected onto each area of the semiconductor substrate where a die is to be formed. Step-and-repeat projection systems frequently have lenses placed between the photomask and the semiconductor substrate such that a pattern projected onto the photoresist is smaller than the pattern of the photomask. Pattern reduction by, e.g., a factor of four or five is common for scanners or steppers, respectively. The printable field size of the lens is often larger than a single die. Typically, a photomask will pattern a portion of the photoresist corresponding to one or more circuits. For example, the photomask may contain patterns for four separate die.

Inherent to each photolithography patterning system, i.e. scanner or stepper, are aberrations which may prevent the system from transferring the photomask pattern exactly as printed on the photomask. An aberration is broadly defined as any deviation of the real performance of a system from its ideal performance. An aberration in a photolithography patterning system may be attributed to any number of factors, e.g., one or more lenses of the system or the stage. Aberrations may be repeatable under similar exposure conditions, therefore they may be mapped for a particular patterning system and process layer. In an area where an unacceptable system aberration is present, the corresponding portion of the photoresist may be improperly patterned, resulting in an incorrect or incomplete photomask pattern transfer onto the photoresist. In either case, the developed photoresist will not have the desired pattern and the photoresist may not protect the proper portions of the underlying semiconductor substrate when the photoresist is used as a mask in subsequent processing. For example, if the photoresist is used to mask a metal layer which will be etched to form interconnects, a defective mask may result in a detrimental electrical performance, such as two interconnects shorting. Or, the defective metal layer mask may result in an interconnect with a width less than that targeted and therefore a current

carrying capacity less than that targeted. Both situations may lead to failure of the resultant integrated circuit. In general, incorrect patterning of photoresist will decrease yields of fabricated integrated circuits and thus increase manufacturing costs.

It is therefore desirable to develop a method to reduce the effects of photolithographic system aberrations. Lessening the effects of these aberrations may allow higher die yields, and may also prolong the useful life of existing photolithographic patterning systems.

DISCLOSURE OF INVENTION

The problems outlined above are in large part addressed by a method in which photomask geometry data is generated to compensate for the aberrations of a photolithography patterning system. A photolithography patterning system is evaluated to characterize its aberrations. Evaluation of the patterning system may be performed, for example, by patterning a semiconductor substrate with a test photomask, thus creating test patterns on the semiconductor substrate. Images of the test patterns may be evaluated to characterize aberrations present in a photolithography patterning system. Aberrations may be attributed to, for example, the illumination source, the lens(es) or the stage of, e.g., an exposure processing step. Characterization of the aberrations will indicate the size and location of an aberration-affected area, and the aberrations' effects on various types of design features.

The characterization of a photolithography patterning system's aberrations may be used to identify which design features will be susceptible to distortion. Design features may be part of an intended integrated circuit pattern for a specific processing layer for one or more die. Design features have dimensions and positions which are proportional to intended substrate feature dimensions and positions. The design features which would be affected by the aberration(s) are modified by changing their size(s) and/or shape(s) to form mask features configured to compensate for the aberration-induced distortions. A photomask having the modified mask features may then produce substrate features having the intended dimensions and positions in the aberration-affected areas, rather than distorted dimensions and positions. The mask features may be included in a set of photomask geometry data.

The photomask geometry data would be stored on some type of carrier or memory medium, i.e. a hard drive. The geometry data would then be transferred to a photomask manufacturing area. A photoblank, such as a quartz plate having one or more opaque materials coated with photoresist, may be exposed using some type of photomask writing tool, i.e. an e-beam or laser system, to create a photomask which uses the photomask geometry data to compensate for aberrations in a photolithography patterning system. The resultant photomask, when used in the characterized patterning system, may have mask features which project substrate features that are proportional to the sizes and positions of (undistorted) design features.

In addition to the method described above, a system is contemplated herein. The system comprises a storage medium containing programming instructions for evaluating patterning system data, thus characterizing aberrations of a photolithography patterning system. The system also comprises programming instructions for modifying design feature data to compensate for aberrations, thus generating mask feature data. The system may further comprise a photolithography patterning system associated with the characterized aberrations, a metrology tool associated with the patterning system data, and/or a photomask writing tool associated with transfer of the mask feature data to a photoblank.

In an alternative embodiment, a system contemplated herein comprises a storage medium containing mask feature data which includes design feature data modified to compensate for aberrations. The storage medium may further comprise the design feature data and/or patterning system data used to characterize the aberrations. The system may further comprise a photolithography patterning system associated with the characterized aberrations, a metrology tool associated with the patterning system data, and/or a photomask writing tool associated with transfer of the mask feature data to a photoblank.

Finally, a photomask is also contemplated herein. The photomask comprises at least one mask feature which has been altered with respect to a corresponding design feature to correct for a patterning system aberration. Specifically, at least one of the mask features on the photomask differs in relative dimensions and/or positions from a corresponding feature found on a semiconductor topography by exposure of the topography through the photomask, where the location of this differing mask feature corresponds to a position affected by an aberration associated with a photolithography patterning system used for the exposure.

BRIEF DESCRIPTION OF DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

Fig. 1 is an exemplary cross-sectional side-view schematic of a photolithographic system for transferring a pattern located on a photomask onto a photoresist layer located on a semiconductor substrate;

Fig. 2 is an exemplary top plan view of a photomask and an upper surface of the semiconductor substrate with circuit patterns affected by an aberration in a photolithographic system;

Fig. 3 is an exemplary plan view of an aberration's effect on a design feature, and a modified mask feature which compensates for the aberration's effect;

Fig. 4 is an exemplary top plan views of a test photomask and an upper surface of the semiconductor substrate with test features;

Fig. 5 is a block diagram of a scanning electron microscope;

Fig. 6 is a flow diagram for an exemplary procedure for generating photolithography patterning system data;

Fig. 7 is a flow diagram for an exemplary procedure for generating photomask geometry data;

Fig. 8 is an exemplary top plan view of a photomask compensated to correct for a photolithographic patterning aberration and an upper surface of a semiconductor substrate patterned on the aberrant patterning system; and

Fig. 9 is a block diagram of a system for compensating for aberrations.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the present invention.

MODE(S) FOR CARRYING OUT THE INVENTION

Turning now to the drawings, Fig. 1 shows an exemplary side-view schematic of a photolithographic system and a portion of a semiconductor substrate on which patterns are being printed. The photolithography patterning systems may include many elements not shown in Fig. 1, e.g., more lenses. Photolithography patterning system 10 is preferably a step and repeat projection system, i.e. a "stepper" or "scanner". Prior to placing a semiconductor substrate in photolithography patterning system 10, photoresist 24 is applied to the semiconductor substrate 22 by, for example, spin coating. When placed in photolithography patterning system 10, semiconductor substrate 22 occupies wafer stage 26. Light source 12 projects light through photomask 16 and lens 20 onto photoresist 24 that is located on an upper surface of semiconductor substrate 22. The light from light source 12 is preferably from the ultraviolet portion of the electromagnetic spectrum. Light source 12 may be, for example, a mercury-vapor lamp or an excimer laser. However, other radiation wavelengths may also be suitable, such as x-ray radiation. Photomask 16 includes clear and opaque regions that define a pattern to be created in photoresist 24. Exposure of portions of photoresist 24 to the light changes the solubility of those portions in a developer. Photomask stage 14 is occupied by a photomask 16. The pattern of photomask 16 may include geometry data which may be used to produce integrated circuit features. The pattern of photomask 16 may also include test patterns which may be used to verify proper operation of photolithography patterning system 10. Lens 20 may reduce the size of the pattern of photomask 16 projected onto photoresist 24 by, for example, a factor of four or five.

When lens 20 reduces the size of the pattern of photomask 16 projected onto photoresist 24, the area of the pattern projected onto photoresist 24 is typically less than the area of semiconductor substrate 22 where patterns of photomask 16 are desired. To project the pattern of photomask 16 onto other portions of photoresist, photolithography patterning system 10 moves, or "steps", wafer stage 26 upon which semiconductor substrate 22 is arranged and projects the pattern onto a different portion of photoresist 24. This procedure is repeated until the pattern has been projected onto all areas of photoresist 24 where a pattern is desired. After every area of photoresist 24 where a pattern is desired has been patterned, the semiconductor substrate 22 is removed from photolithography patterning system 10, and the pattern printed on photoresist 24 is typically developed by spraying developer onto photoresist 24. For example, if photoresist 24 is a positive photoresist, the developer removes portions of photoresist 24 that have been exposed to light by photolithographic system 10. If photolithography patterning system 10 has an aberration, portions of photoresist 24 may be improperly defined due to the aberration. Improper definition may result in improper transfer of the pattern of photomask 16 onto photoresist 24 and may ultimately lead to failure of the integrated circuit being fabricated. An aberration of patterning system 10 is any deviation of the real performance of the patterning system from its ideal performance. An aberration may result from a localized defect on an optical component of the photolithography patterning system, for example, the lens 20. Some circumstances that may produce a lens aberration include incorrect lens construction (i.e. incorrect shape or thickness of glass elements) or improper lens use (i.e. incorrect environmental conditions). Also, an aberration may result from a localized defect of a physical component of the photolithography patterning system, for example, inconsistent movement of the wafer stage 26, or alternatively, localized defects of a consistently moved stage.

Fig. 2 depicts an improper transfer of a pattern from a photomask 30 onto a wafer surface 40 due to a photolithography patterning system aberration. Integrated circuit photomask 30 is shown in Fig. 2a with patterns

for four separate yet identical die regions, 32a, 34a, 36a, and 38a. When photomask 30 is used in a photolithography patterning system, the patterns for all four circuits 32, 34, 36, and 38 are transferred to the wafer 40 each time the photolithography patterning system "steps" the wafer and exposes the wafer surface. Wafer 40 is shown in Fig. 2b with multiple patterns of photomask 30. Fig 2c and 2d each illustrate one of the projections of photomask 30 transferred to the wafer 40. The patterns of circuits 32c, 32d, 34c, 34d, 38c, and 38d have each transferred properly. However, the circuits 36c and 36d have each transferred improperly, and thus may not function as designed. Further, each image of circuit 36 projected to wafer 40 has also transferred improperly due to the system aberration affecting the exposure of the portion of photomask 30 containing circuit pattern 36.

Fig. 3 illustrates the approach of the method described herein to compensate for aberrations. Fig. 3a illustrates a portion of a desired design feature 50 as it may appear, for example, on a screen of a Computer Aided Design ("CAD") system. Area 51 indicates an area of feature 50 corresponding to an area of a corresponding photomask having exposure distorted by a patterning system aberration. Fig. 3b illustrates an exemplary distorted substrate feature 52 obtained from a photomask with a mask feature having the same relative size and position as the design feature 50 when a projection of this feature is coincident with aberration-affected area 51. Fig. 3c illustrates an exemplary mask feature 54 derived from a modification of design feature 50 which has incorporated compensation for the aberration-affected area 51. Fig. 3d illustrates a compensated substrate feature 56 obtained from mask feature 54 when a projection of mask feature 54 is coincident with the aberration-affected area 51. Compensated substrate feature 56 has pattern features with the same relative size and position as the desired design feature 50. It is noted that the geometries shown in Fig. 3 are for general illustrative purposes only, and don't necessarily represent an actual distortion/correction pair. The method described herein allows the manufacture of substrate features which have the same relative sizes and positions as desired design features despite the presence of photolithography patterning system aberrations.

In order to compensate for system aberrations, detailed analysis of the performance of a photolithography patterning system is required. System aberrations may be detected and characterized without the aid of patterning test patterns. For example, through-the-lens interferometric ("TTLI") analysis or direct aerial image measurement ("DAIM") may be utilized to characterize system aberrations. However, in a preferred embodiment, characterization via test patterns is used. Fig. 4a illustrates a test photomask 42 which may be used to analyze the performance of a photolithography patterning system. Test photomask 42 may contain a plurality of pattern areas 43 each having a plurality of features 44 patterned on a topography using the same optical system that applies production features onto a customer-destined die. In a preferred embodiment, the features 44 will include lines at the minimum allowable feature size printable by photolithography patterning system 10. The minimum allowable feature size may be, for example, 0.18 μm. The pattern area 43 may contain either dense lines and/or isolated lines, and may contain either horizontal and/or vertical lines. The pattern area 43 may also contain posts, vias, or other structures.

Fig. 4b illustrates a test wafer 46 which may be used to analyze the performance of a photolithography patterning system. In a preferred embodiment, the pattern of test photomask 42 is projected onto the surface of a wafer 46 multiple times using photolithography patterning system 10 and subsequently developed to form features 48 on wafer 46. Exposure region 47 represents the pattern transferred from photomask 42 with a single exposure. In a preferred embodiment, the exposure region 47 will span the entire printable field area of

photolithography patterning system 10. The exposure region 47 may be transferred to the entire surface of wafer 46 or may be transferred to only one or more areas of the wafer surface. Exposure region 47 may contain a plurality of pattern regions 49. Pattern region 49 represents the pattern transferred from pattern area 43. Within pattern region 49 is a plurality of test features 48. In a preferred embodiment, images of the test features 48 are analyzed to determine the presence of system aberrations. System aberrations may indicate that test features 48 in the area of an aberration are distorted in such a way that an integrated circuit having the distorted feature would not function optimally. Alternatively, a system aberration may indicate that the cosmetic appearance of completed integrated circuits in the area of the aberration would be such that customers who purchase the completed integrated circuits will be dissatisfied. For example, a "cosmetic" defect may be suspected of contributing to an as yet unidentified future functional defect.

Since the test features are relatively small (for example, less than 0.25 μm), examination of the test features requires some form of magnification. The test patterns 48 on the wafer surface are examined by a metrology tool, for example, a scanning electron microscope, an optical microscope, a laser confocal imaging system, or a profilometer. In a preferred embodiment, the device for magnifying the test patterns is a scanning electron microscope which uses a focused electron beam to create a magnified image of a surface. Fig. 5 depicts a cross-sectional side-view schematic of a scanning electron microscope 60. Scanning electron microscope 60 is enclosed by vacuum chamber 62. Load lock 64 allows semiconductor substrate 22 to be introduced into vacuum chamber 62 and placed on stage 70. Electron column 66 generates a focused electron beam and deflection system 68 may raster the electron beam across a portion of semiconductor substrate 22. Typical electron beam energies may range from approximately 0.5 to 40 keV. Secondary electrons emitted from the surface of semiconductor substrate 22 are detected by detector 72. The output of detector 72 is used to modify an intensity of the image as a function of electron beam location. Images of the surface magnified by a factor of 10 to 100,000 are typically produced by scanning electron microscopes. Deflection system 68 is typically able to raster the electron beam over a limited area of semiconductor substrate 22 such that only a portion of semiconductor substrate 22 is within a field of view of scanning electron microscope 60. To image other portions of semiconductor substrate 22, stage 70 may move semiconductor substrate 22 to bring different portions of semiconductor substrate 22 underneath deflection system 68 and within the field of view of scanning electron microscope 60.

Fig. 6 shows a flow diagram for a procedure for characterizing aberrations of a photolithography patterning system according to some embodiments of the method recited herein. Initially, images of test patterns on a semiconductor substrate are evaluated using a metrology tool, e.g., measured using a scanning electron microscope (box 80). The metrology tool may be under the control of a computer system. The images measured by the scanning electron microscope are then sent to a computer system (box 82). The computer system then stores a copy of the image in an appropriate storage medium such as a hard disk (box 84). Once the computer system has received the images of the test patterns, the computer system may assess the images to determine whether the patterned image is acceptable or unacceptable (box 86). In one embodiment, the computer system may compare the measured images of each test pattern to a reference image of the test pattern. The computer system calculates the difference between the measured images and the reference image. The differences are predetermined to be either acceptable or unacceptable. If a difference is determined to be unacceptable, the computer system finds a function that converts the unacceptable measured image into an acceptable image. This

function may be selected from a set of predetermined functions. The conversion function may be stored with location information from the unacceptable measured image to generate photolithography patterning system aberration data (box 88). In such an embodiment, the patterning system data may include functions useful in compensating for the aberration's effect on various design features. Alternatively, the patterning system aberration data may principally include a function representing the optical field distribution corresponding to the aberration, with specific compensation functions included in a different set of data. The process of determining aberration data may be repeated a multiplicity of times to ensure a degree of statistical significance. Additionally, it may be desirable to generate aberration data for a particular patterning system by using multiple test photomasks and/or a multiplicity of test features.

The aberration data may then be combined with design feature data, such as that containing design feature 50 of Fig. 3a, to create photomask geometry data including corrected mask features. A photomask created with such corrected mask features may have inherent corrections for a particular photolithographic system. Fig. 7 depicts a flow diagram for generating photomask geometry data according to one of the embodiments of the method recited herein. Initially, as described above, aberrations of a photolithography patterning system are characterized, and the data from this characterization is provided (box 120). The characterization may include the locations of aberrations in the system, the area affected by each aberration, and specific effects of each aberration on every type of design feature analyzed. For example, a particular aberration may cause distortion to a via, but not to a line. Next, the design feature data (box 122) will be compared to the characterization data. The two datasets will be analyzed together to determine which, if any, design features will be affected by the characterized aberrations. This analysis may, for example, be performed on a computer aided design system which could overlay the aberration data with the design feature data to illustrate graphically the potential effects of the patterning system aberrations. Once analysis has been performed, the design feature data may be modified to create mask feature data which compensates for the aberrations (box 124). Suitable modifications may include, e.g., changing the width or curvature of a feature.

Design feature data modification may compensate for local aberrations in such a manner that multiple copies of identically designed integrated circuits on the same photomask may not have the same mask features. Additionally, such modification may compensate for systemic aberrations of a specific photolithography patterning system such that multiple photomasks of identically designed integrated circuits intended for use on different like-model photolithography patterning systems may not have the same mask features. Accordingly, the mask features may differ from those found on existing photomasks which have mask features that are not proportional to desired substrate features, such as Optical Proximity Correction ("OPC") photomasks or phase shift photomasks. The mask features which compensate for aberrations may also be incorporated into OPC and/or phase shift photomasks. An OPC photomask contains tiny serifs on the corners of features and in the corners of features to help compensate for "lost" light which tends to round the corners, and a phase shift photomask contains enhancements that selectively alter the phase of the light to take advantage of destructive interference to improve resolution and depth of focus. Neither OPC photomasks nor phase shift photomasks are designed to overcome the particular system aberrations of individual photolithography patterning systems. Finally, the mask features are included in photomask geometry data (box 126) and saved on a storage medium. Photomask geometry data is suitable for transmission to a mask-making area or facility. Typically, further formatting will be required to before a photomask is created by a photomask writing tool, i.e. an e-beam or laser.

Formatted data may include photomask geometry data which has been fractured, that is, translated into a language the write tool can understand. The write systems typically use rectangles and trapezoids, so the photomask geometry data is divided up, or fractured, into these shapes. The formatted data may also include fiducials or other reference marks, and/or instructions for the placement of all the different patterns on the photomask.

The formatted data is transferred to a photomask writing tool to create a photomask. The photomask writing tool, e.g., an e-beam or laser system, will write the data to a photoblank to create a compensated photomask. Fig. 8 illustrates a compensated photomask 90 and resultant substrate features on wafer surface 100. Compensated photomask 90 is shown in Fig. 8a including patterns for four separate circuits, 92a, 94a, 96a, and 98a. The four circuits are intended to be identical on the wafer surface. However, as was illustrated in Fig. 2, an aberration exists in the photolithography patterning system which affects the exposure of the portion of the photomask containing circuit 36. The corresponding portion of the compensated photomask contains the pattern for circuit 96. As such, the pattern for circuit 96 has been compensated to correct for the aberration. Note that the circuit 96a shown on photomask 90 has a feature which is larger than the corresponding features shown in circuits 92a, 94a, and 98a. However, note that the patterns 96c and 96d are essentially identical to the corresponding patterns of circuits 92c, 92d, 94c, 94d, 98c and 98d shown in Figs. 8c and 8d on wafer 100. Further, each image of circuit 96 projected to wafer 100 has also transferred correctly due to the compensated photomask 90. It is noted that the feature shapes shown in Fig. 8 are merely exemplary, and that actual compensating masks may include alterations of many parameters, such as linewidth, curvature, shape, or thickness.

Fig. 9 depicts an embodiment of system 90 for compensating photolithography patterning system aberrations. Fig. 9 illustrates the functionality, and not necessarily the specific structure, of the system. Included within the system 90 is storage medium 94. Storage medium 94 may take many forms. It may be a volatile or non-volatile memory (e.g., read-only memory or random access memory), a magnetic or optical disk, a magnetic tape, or a transmission path. Storage medium 94 includes programming instructions 96 for evaluating photolithography patterning system data and programming instructions 98 for modifying design feature data. Also included within storage medium 94 may be mask feature data 100 and photomask geometry data 102. Storage medium 94 may be a singular storage medium, or it may be a plurality of storage mediums. Storage medium 94 is accessible by a computer system such as computer system 92 but may not actually be included within the computer system as shown in Fig. 9. Computer system 92 may be a singular processing system, or it may be a plurality of processing systems. Photolithography patterning system 10, also shown above in Fig. 1, may be included in system 90. System 90 may also comprise mask writing tool 106, CAD system 108 and/or metrology tool 60. An embodiment of metrology tool 60 is also shown in Fig. 5.

INDUSTRIAL APPLICABILITY

This invention is suitable for a number of industrial applications including, but not limited to, the fields of integrated circuit manufacture. It will be appreciated to those skilled in the art having the benefit of this disclosure that this invention is believed to provide a method, system, and photomask for compensating photolithography patterning system aberrations. The system or method compensates for aberrations by evaluating patterning system data and thereafter modifying design features to thereby produce a

photolithography mash which can compensate for such aberrations. Further modifications and alternative embodiments of various aspects of the invention will be apparent to those skilled in the art in view of this description. For example, this invention would apply not only to semiconductor manufacturing, but also to any microlithography application, e.g., printed circuit board manufacturing. It is intended that the following claims be interpreted to embrace all such modifications and changes and, accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

WHAT IS CLAIMED IS:

1. A system for compensating aberrations associated with a photolithography patterning system, characterized in that the system includes a storage medium and wherein said storage medium comprises mask feature data, said mask feature data comprising design feature data modified to compensate for aberrations characterized by photolithography patterning system data.

2. The system as recited in claim 1, wherein the storage medium further includes:

first programming instructions executable on a computer system to evaluate patterning system data and characterize aberrations associated with the photolithography patterning system, and

second programming instructions executable on the computer system to modify design feature data and compensate for the aberrations, such that mask feature data can be produced.

3. The system as recited in claim 2, wherein the patterning system data comprises test pattern images.

4. The system as recited in claim 3, wherein the aberrations are characterized by comparing each of the test pattern images to a reference image.

5. The system as recited in claim 3, wherein said characterizing aberrations comprises comparing an image of a first test pattern to images of subsequent test patterns.

6. A method to compensate for aberrations in a photolithography patterning system, said method comprising:

identifying design features which are susceptible to distortion by one or more characterized aberrations of the photolithography patterning system, wherein design feature dimensions and positions are proportional to intended substrate feature dimensions and positions; and

generating photomask geometry data, wherein the data comprises mask features incorporating compensation for effects of aberrations on the susceptible design features, and wherein said mask features are suitable for transfer to a photoblank such that the resultant photomask produces substrate features having reduced aberration-induced distortion.

7. The method as recited in claim 6, further comprising transferring said mask features to a photoblank.

8. The method as recited in claim 6, further comprising characterizing the aberrations associated with the photolithography patterning system.

9. The method as recited in claim 6, further comprising storing the photomask geometry data on a storage medium.

10. A photomask, comprising multiple mask features wherein at least one of the mask features differs in relative dimensions and/or positions from a corresponding feature formed upon a semiconductor topography by exposure of the topography through the photomask, and wherein a location within the photomask of said differing mask feature corresponds to a position affected by an aberration associated with a photolithography patterning system used for said exposure.

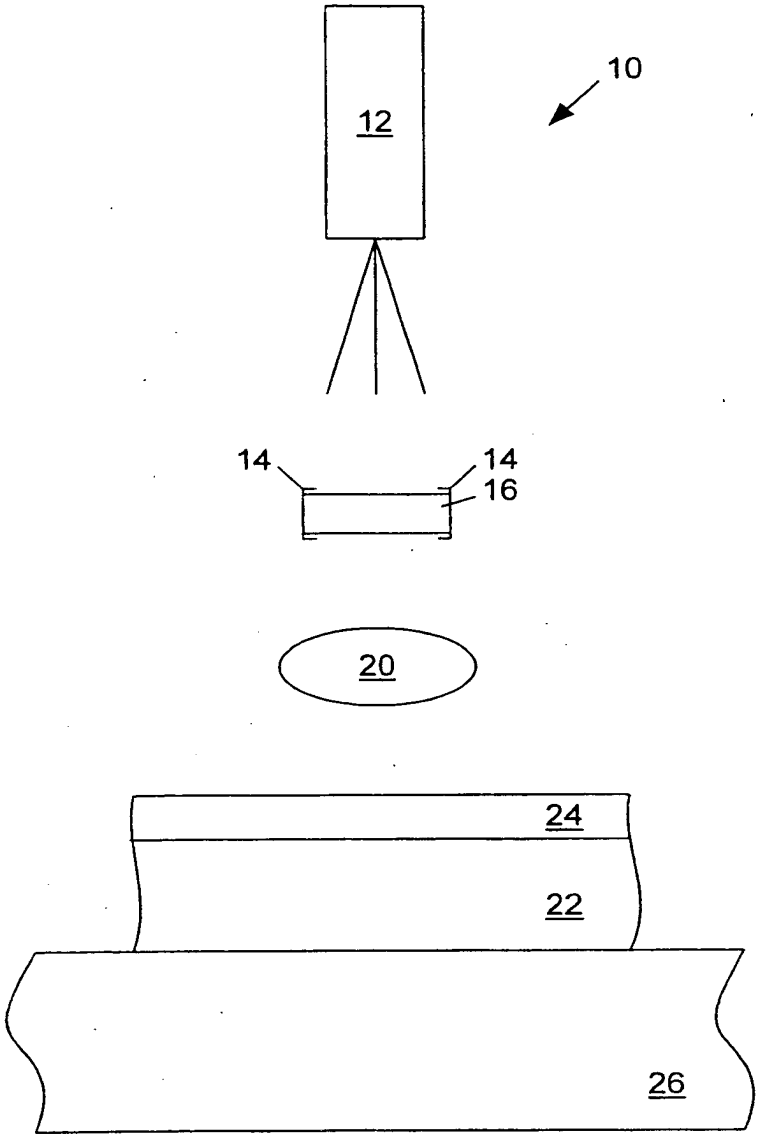

Fig. 1

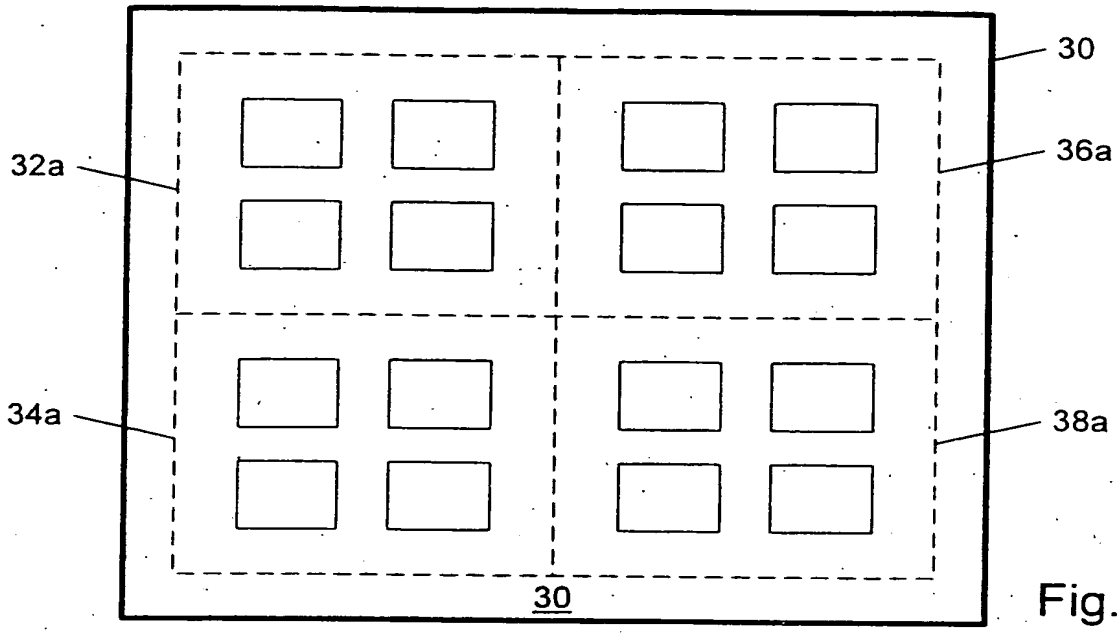

Fig. 2a

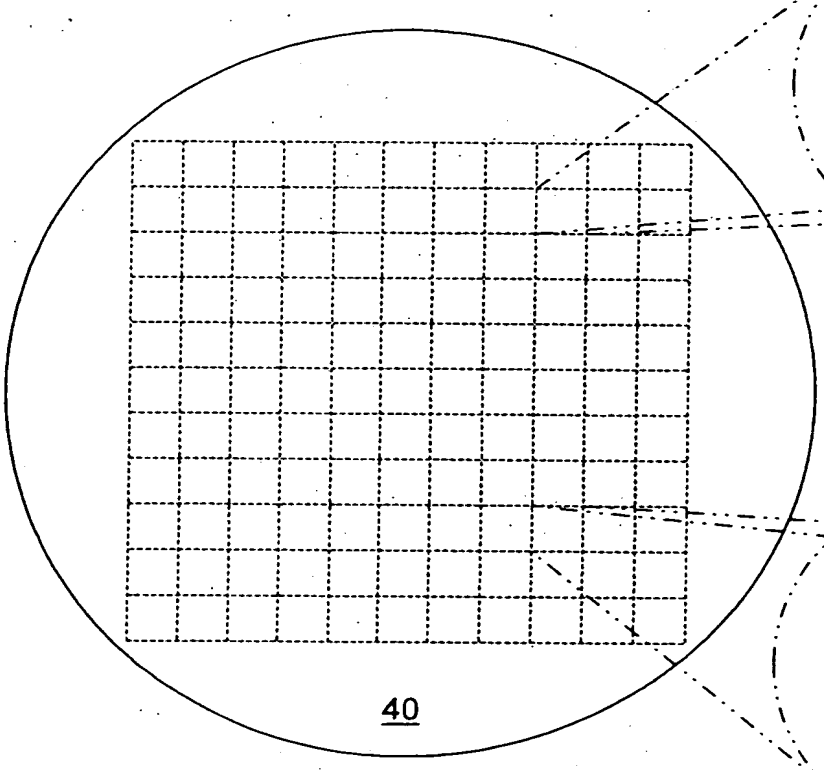

Fig. 2b

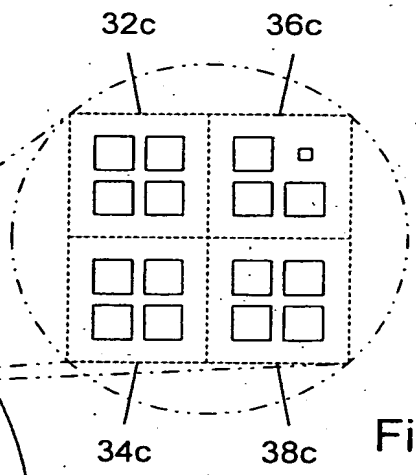

Fig. 2c

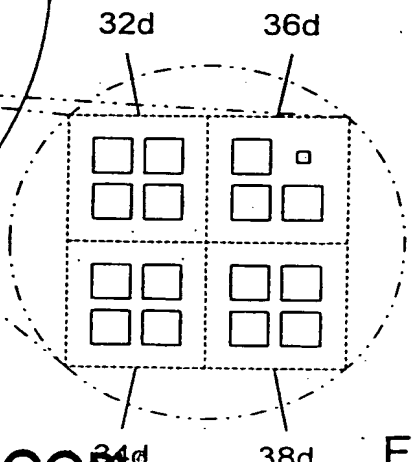

Fig. 2d

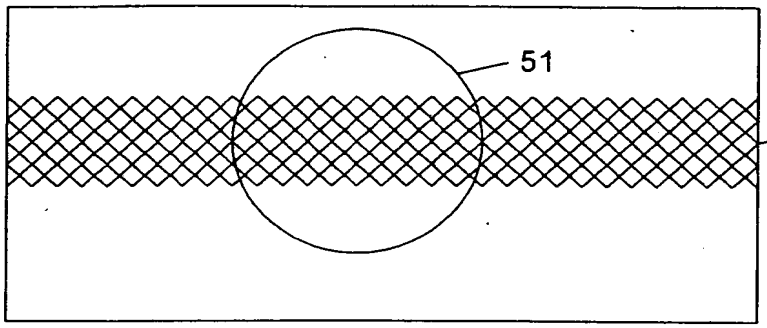

Fig. 3a

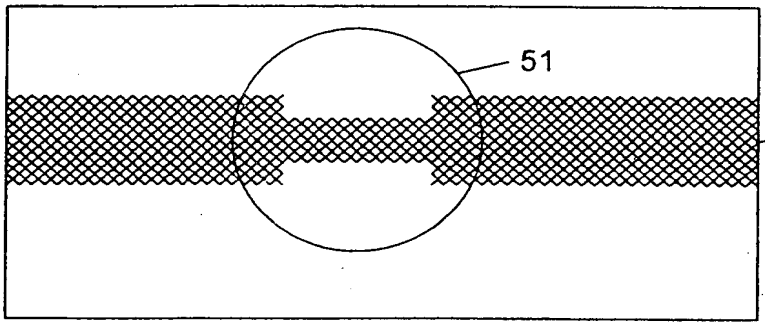

Fig. 3b

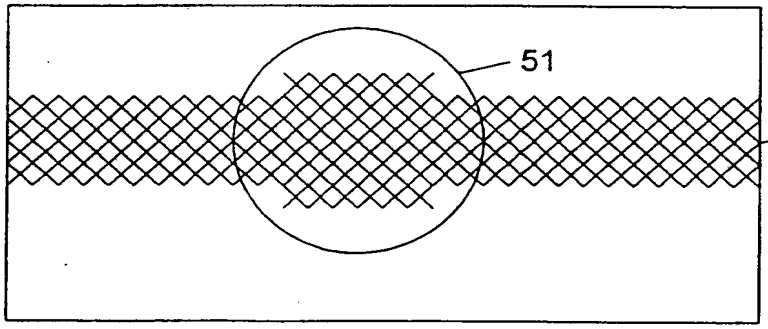

Fig. 3c

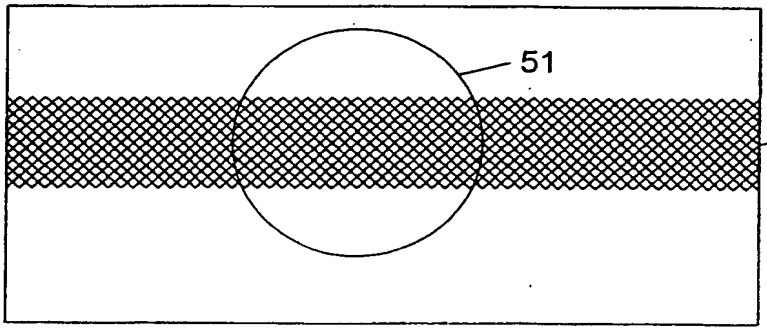

Fig. 3d

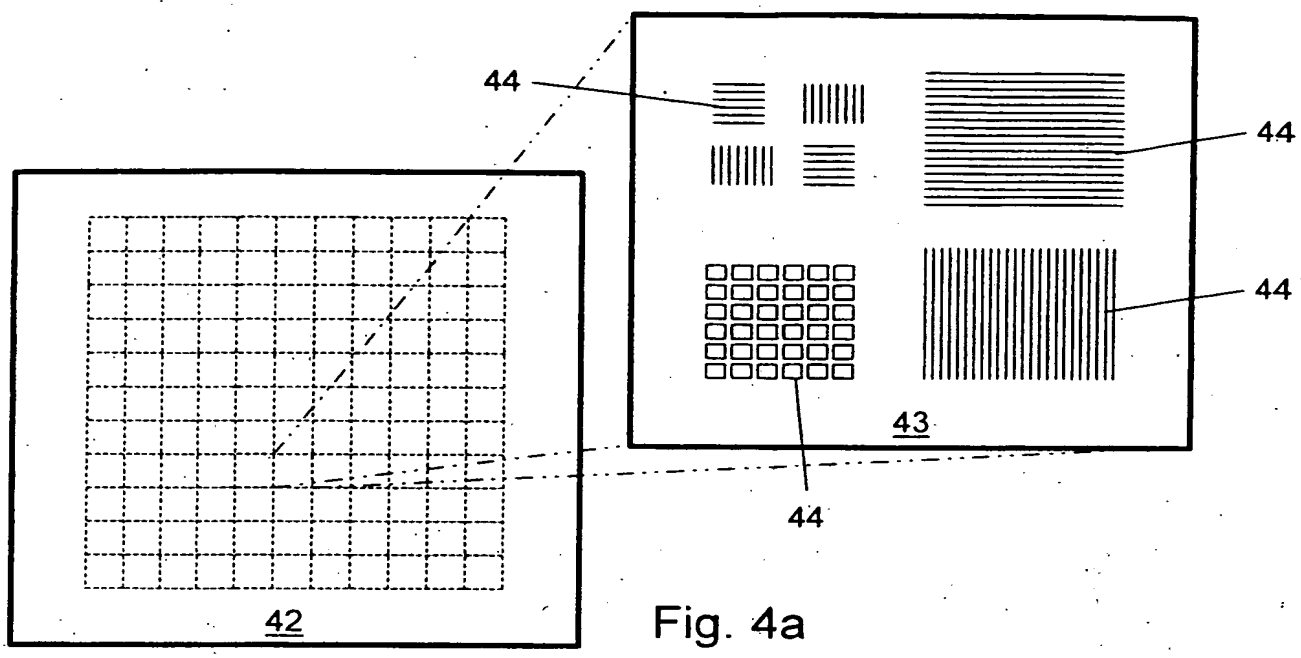

Fig. 4a

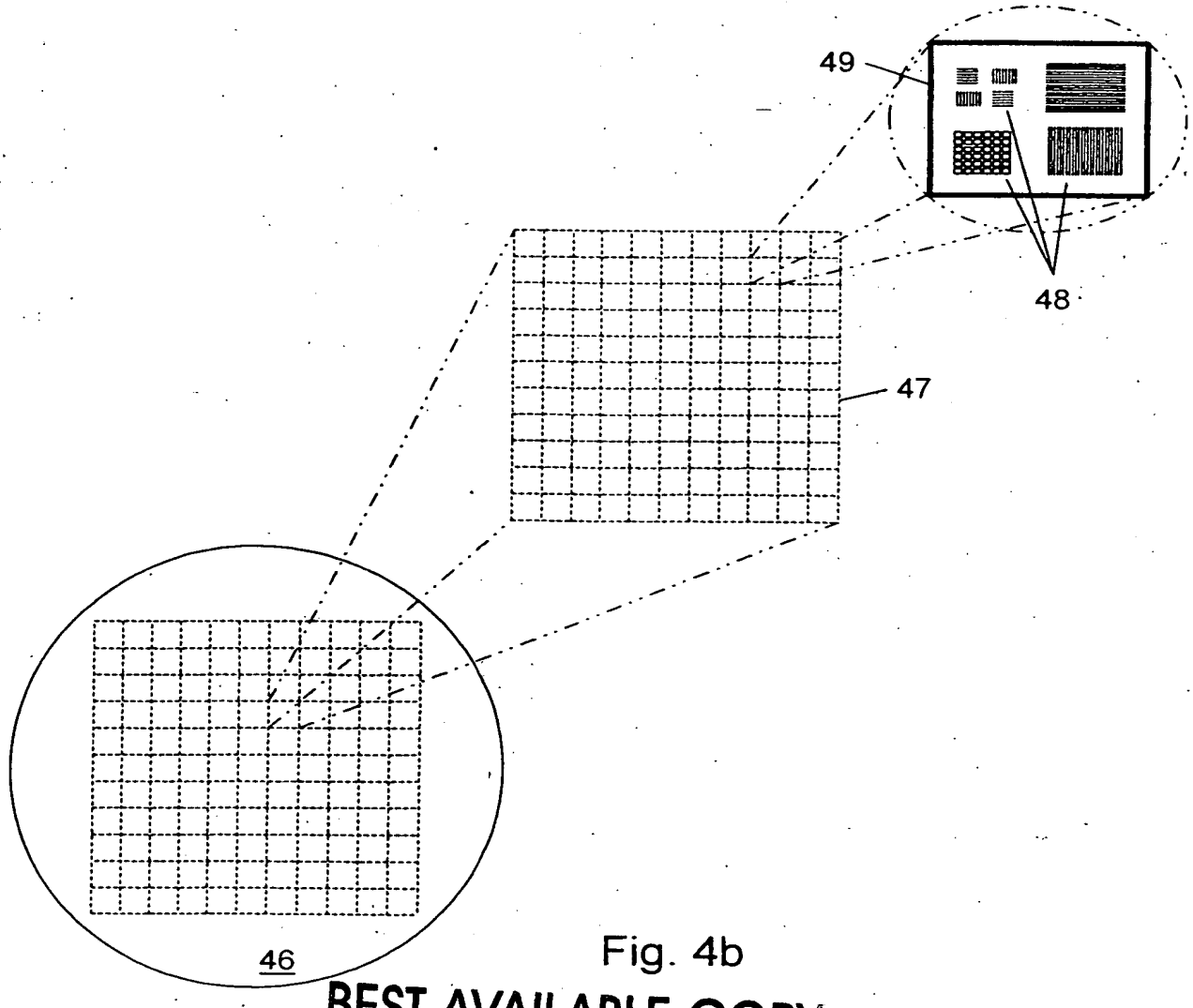

Fig. 4b

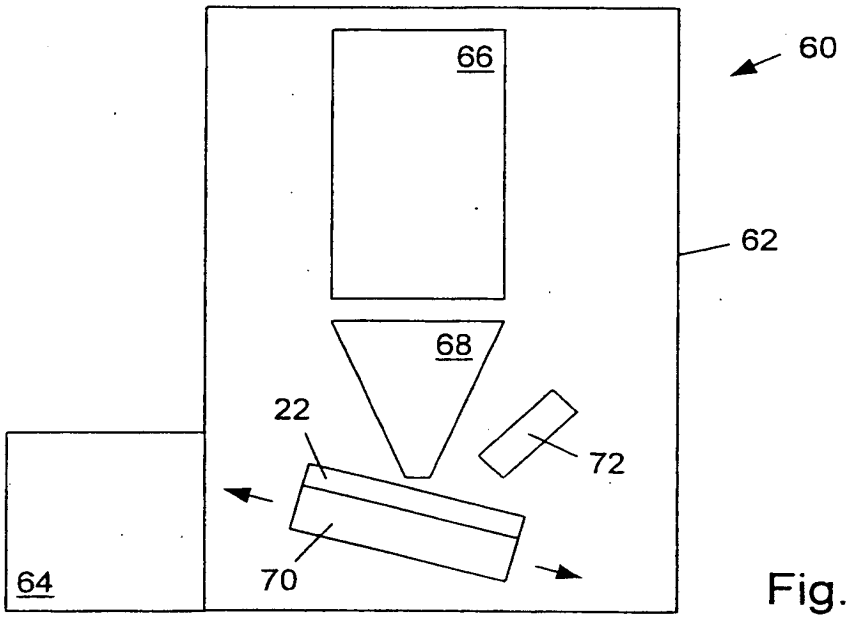

Fig. 5

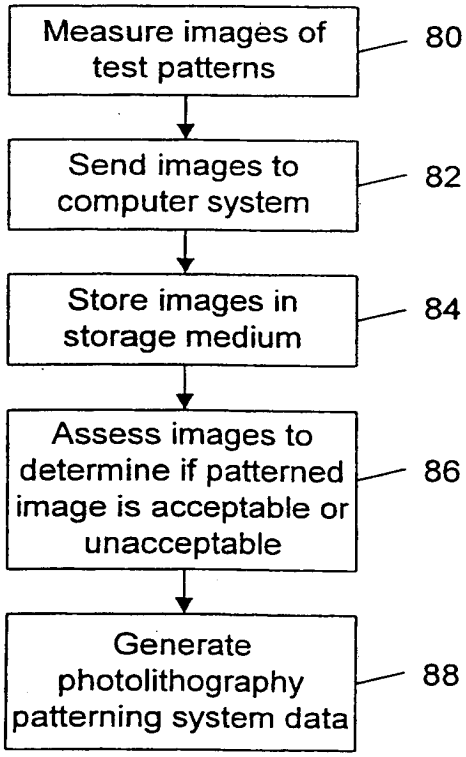

Fig. 6

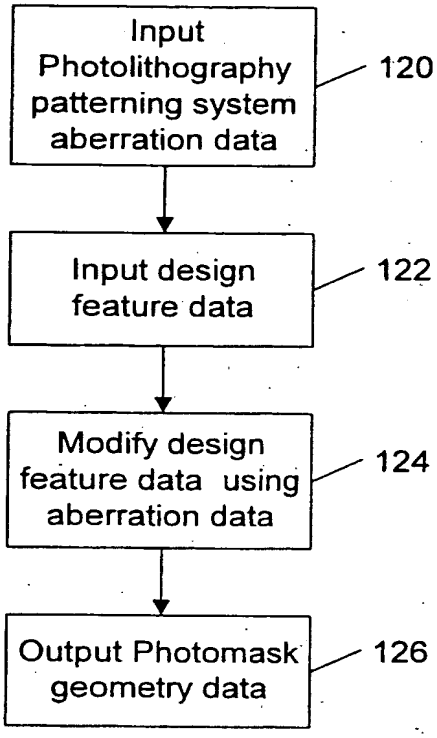

Fig. 7

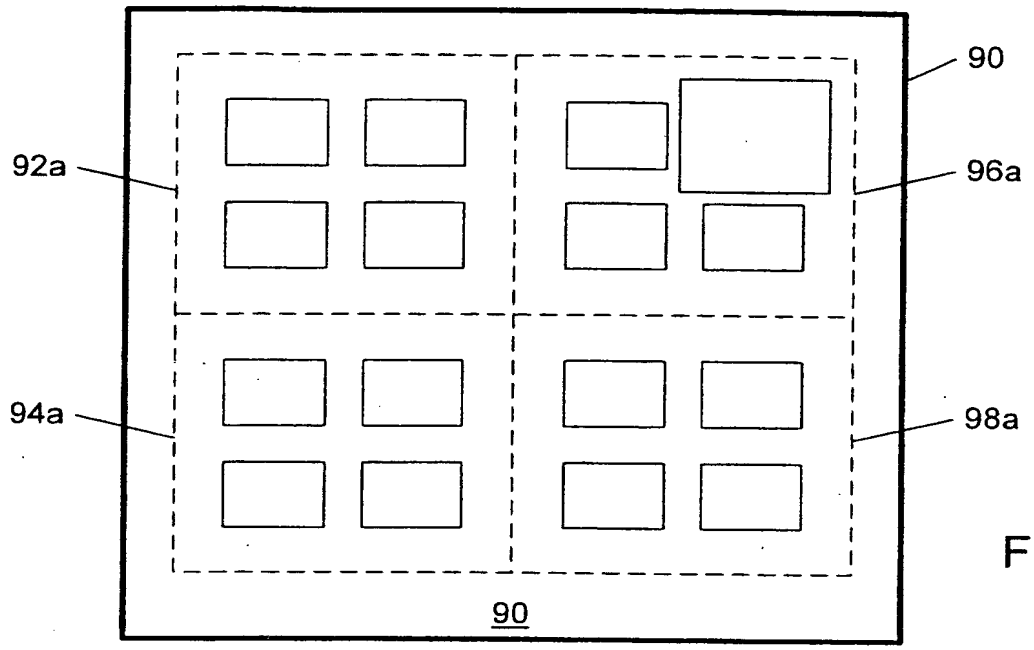

Fig. 8a

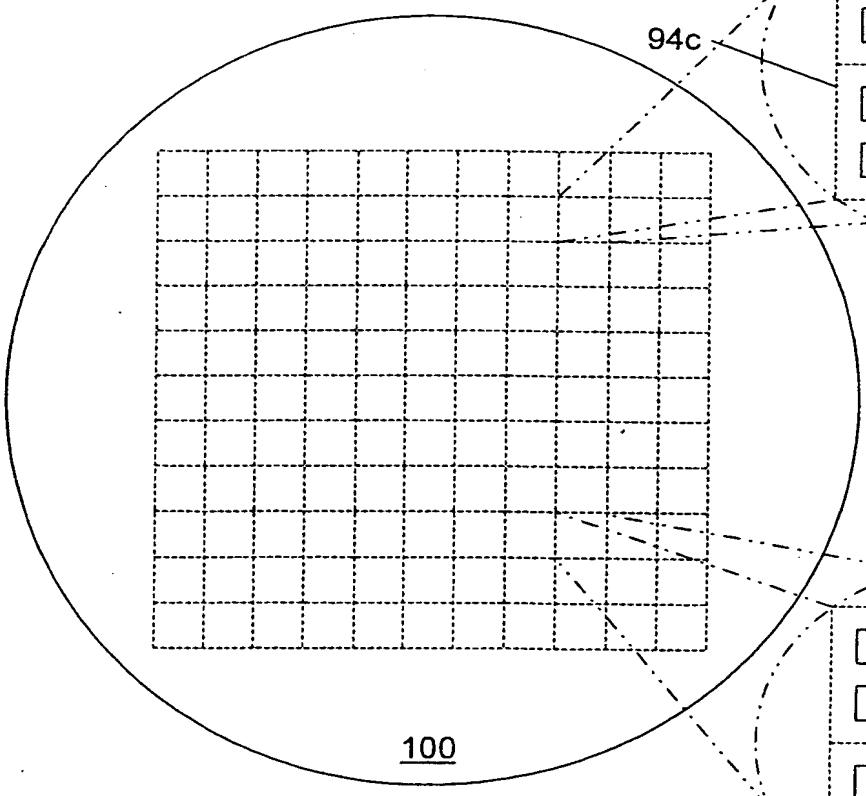

Fig. 8b

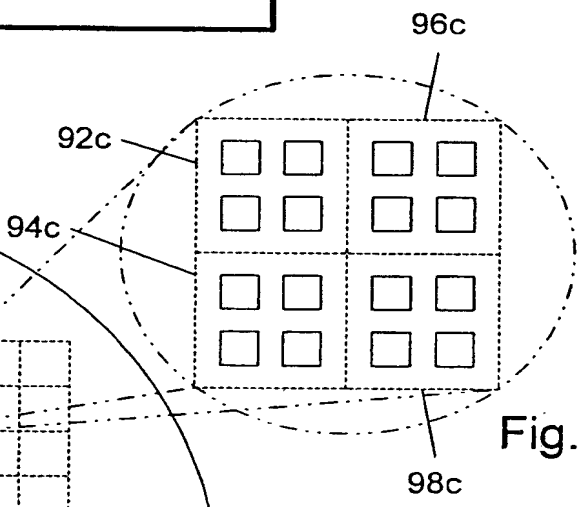

Fig. 8c

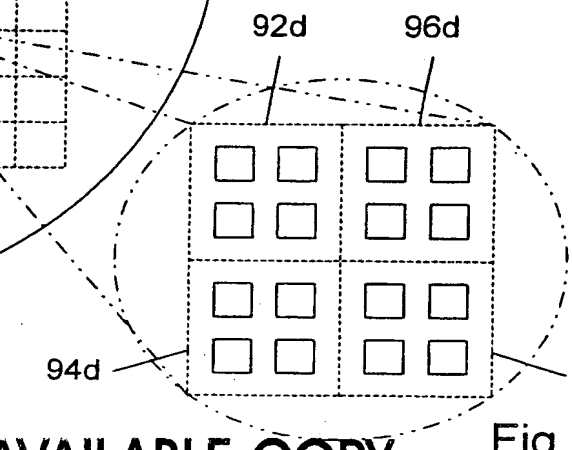

Fig. 8d

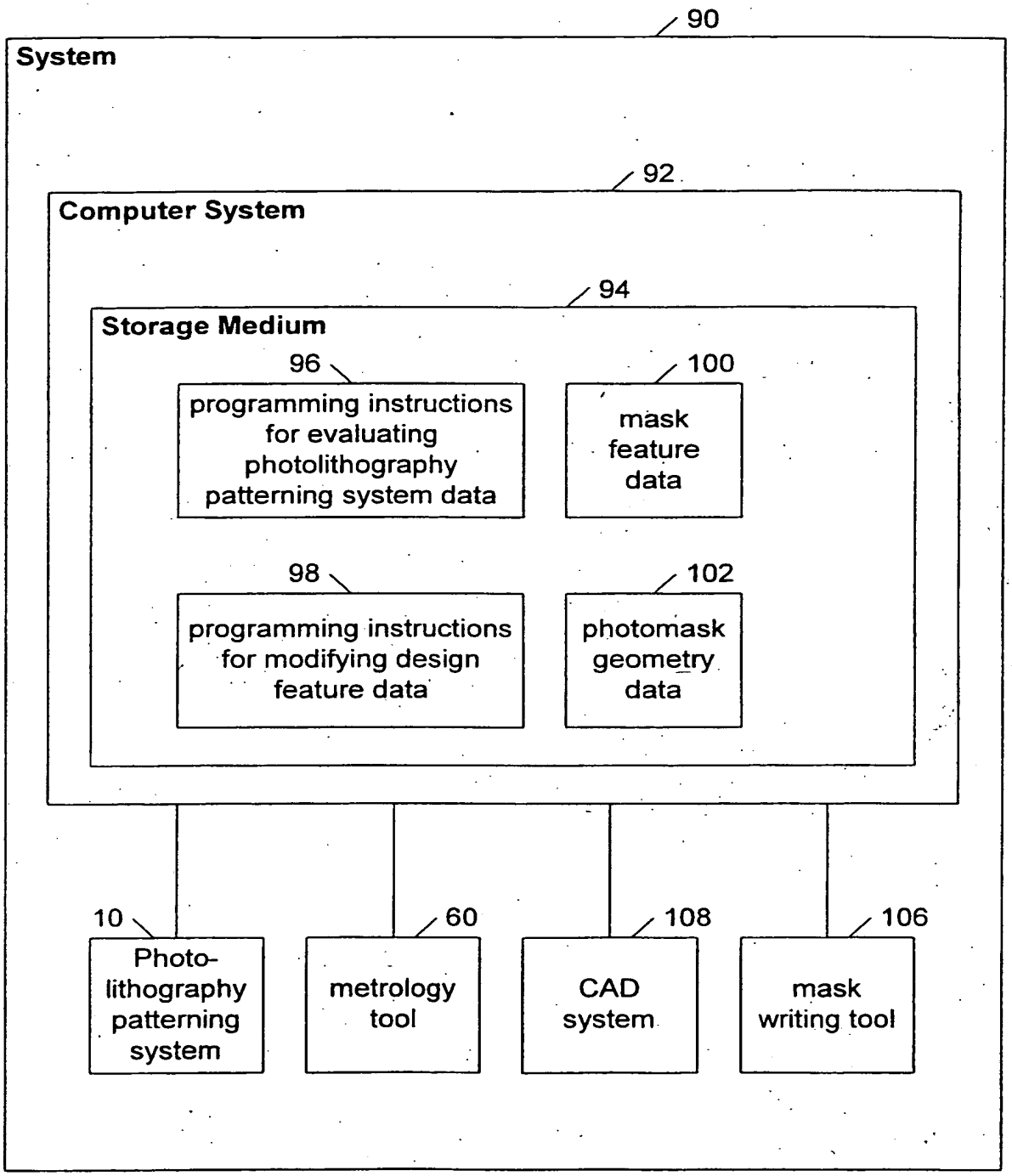

Fig. 9

INTERNATIONAL SEARCH REPORT

Inter onal Application No
PCT/US 00/24932

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G03F7/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 307 726 A (MOTOROLA INC) 22 March 1989 (1989-03-22) column 3, line 6 -column 5, line 17; figures	1-10
X	US 6 014 456 A (TSUDAKA KEISUKE) 11 January 2000 (2000-01-11) abstract; figures 1-3,6	1-10
X	US 5 917 932 A (HARTLEY JOHN GEORGE) 29 June 1999 (1999-06-29) abstract; figures	1-10
X	US 5 308 991 A (KAPLAN SHAY) 3 May 1994 (1994-05-03) abstract; figures	1-10

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[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 November 2000	16/11/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Heryet, C

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INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/US 00/24932

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 4 621 371 A (GOTOU MINEO ET AL) 4 November 1986 (1986-11-04) abstract; figures	1-10
X	WO 99 00828 A (HITACHI LTD ;MURAI FUMIO (JP); SATO KAZUHIKO (JP); HASEGAWA NORIO) 7 January 1999 (1999-01-07) abstract; figures	1-10
X	WO 98 25182 A (ADVANCED MICRO DEVICES INC) 11 June 1998 (1998-06-11) abstract; figures	1-10
X	ITO T ET AL: "Photo-projection image distortion correction for a 1- mu m pattern process" ELECTRONICS & COMMUNICATIONS IN JAPAN, PART II - ELECTRONICS,US,SCRIPTA TECHNICA. NEW YORK, vol. 69, no. 3, PART 02, 1986, pages 30-38, XP002112083 ISSN: 8756-663X abstract; figures	1-10

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter ›nal Application No
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